



## AX1001 8-bit CMOS Microcontroller

### AX1001 Microcontroller Features:

#### CPU Features

- High performance 8-bit RISC-based CPU (DC-100MHz)
- Harvard Architecture
- 33 millions MAC (MMAC) per second (16-bitx16-bit) and 41-bit Addition/Subtraction @ 100MHz
- Compact instruction set. A total of 60 instructions
- All instructions are single-cycled except branch instructions, special I-instructions and MAC instructions
- Special I-Instruction for memory access
  - IREAD: Fast Table lookup capability through run-time readable code in instruction memory, OTP program memory and external memory
  - IWRITE: Real time instruction write to either instruction memory or external program memory
  - ICOPY: Real time instruction copy from instruction ROM (OTP) to instruction RAM using direct memory access
- Fast interrupt response. 30ns internal interrupt response at 100MHz
- 8MBytes External SRAM/FLASH/ROM up to 100MIPS
- Support direct memory access for the following modes:
  - 2KB Data memory to external memory and vice versa
  - 8KB Instruction memory to external memory and vice versa
  - OTP memory to Instruction memory
  - 2KB Data memory to USB FIFO and vice versa
- Sixteen level deep hardware stack for subroutine linkage
- Support software stack
- Deterministic Timing. Use fix number of clocks to execute DSP like instruction
- Multiple sources of interrupt capability

#### Peripheral Features

- Full Speed USB 2.0 device controller and PHY module with DMA
- Two programmable SerDes module supports I<sup>2</sup>C, SPI, UART, MicroWire, Two-wire, Smart Card, Modem and many other serial interfaces
- Hardware GPSI interface
- Four hardware Linear Feedback Shift Register (LFSR) units for CRC, data scrambling, and encryption generation/checking
- 32.768KHz 32-bit real time clock counter/timer with 16-bit prescaler
- Hardware matrix unit for data row/column rotation
- Built-in multi-purpose flip flops MUXed with Port I and Port J
- Timer0: 8-bit timer/counter with 12-bit prescaler
- Timer1: 16-bit timer/counter with 12-bit prescaler can be incremented during SLEEP via external crystal/clock
- Timer2: 8-bit timer with 8-bit period register, 12-bit prescaler and 4-bit postscaler and two 10-bit PWM
- Timer0/Timer1/Timer2 supporting:
  - ☞ Timer mode
  - ☞ Counter mode
  - ☞ Capture/Compare/PWM mode
- Watchdog Timer with on-chip 16KHz RC oscillator
- Analog Comparator module
- Power-On Reset
- Brown-Out Reset
- Multi-Input Wakeup logic on Port A, B and C pins & USB port

### **Memory**

- Low power CMOS One-Time-Programming (OTP) technology
- 16KBytes of OTP Program Memory
- 8KBytes Program/Data Memory (SRAM)
- 2Kbytes of Data Memory (SRAM)
- Support external parallel memory program execution up to 8MBytes
- Support Direct, Semi-Direct and Indirect addressing modes
- Strong program code protection
- All registers are memory-mapped

### **Frequency and Power management**

- Dual oscillator clocks (32KHz and 1-20MHz)
- Real time system clock frequency change in 4 clocks (125Hz-130MHz)
- Provide two power saving modes: stop clock mode and sleep mode
- 2.5V/3.3V VCC and 2.5V/3.3V/5V I/O tolerant

### **Interrupt Capability**

- Timer0, Timer1 and Timer2 overflow interrupt capability
- Watchdog Timer overflow interrupt capability
- External wakeup / interrupt capability on Port A, B and C (8 pins on each port)
- SERDES interrupt capability
- USB interrupt capability
- DMA interrupt capability
- GPSI interrupt capability

### **Flexible I/O**

- 88 GPIO (Notes: Different package has different number of I/O)
- All pins can be individually programmable as I/O
- Inputs are TTL level
- All pins are internal pull-up and pull-down selectable
- All ports have Schmitt Trigger input
- All ports have slew rate control to reduce VDD and GND bounce
- Programmable Sink/Source Current with values of 2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 16mA and 24mA
- Timer0/Timer1/Timer2 MUXed with Port B, Port C, Port D to support Capture/Compare/PWM mode.
- SerDes MUXed with Port A to support I<sup>2</sup>C, UART, SPI master/slave mode
- Analog comparator support on Port A and Port C (RC3 COUT, RA6 INP, RA7 INN)
- GPSI interface MUXed with Port K
- External memory interface MUXed with Port D, E, F, G and Port H

### **Packages**

- 52-pin QFP
- 64-pin LQFP
- 128-pin QFP

### **Programming and Debugging Support**

- On-chip In-System debugging support
- On-chip In-System Serial Programming via two dedicated pins: ISPDP1 pin, ISPDP2 pin. High voltage pin V<sub>PP</sub> is used for high voltage programming voltage