



AX3003 Digital Photo Frame SoC



High Performance 32-bit RISC CPU

- Maximum 120MIPS
- 25 interrupt sources with two priority levels
- Debug interface connects to GDB via JTAG
- Internal 32-bit ticker-tick timer

Program Memory and Data Memory

- 96K Bytes internal SRAM
- 12K Bytes ROM

Flexible I/O

- 112 IO pins
- Configurable internal pull-up
- Configurable slew rate

Timers

- Four 16-bit multi-function timers
- Counter mode
- Capture mode
- PWM mode

General Purpose DMA

- 7 general purpose DMA channels
- 3 LCD DMA channels

16-bit DSP Engine

- 16-bit add (ADD)
- 16-bit subtract (SUB)
- 16-bit signed multiply (MUL)
- 16-bit multiply and accumulate to 40-bit (MAC)
- 16-bit signed multiply and subtract to 40-bit (MAS)

JPEG Decoder

- Sequential
- 8-bit sample within each component
- Huffman coding: 2 AC and 2 DC tables
- Decoder can process 3 components
- YUV-to-RGB converter

Cyclic Redundancy Check (CRC)

- CRC-CCITT
- IEEE 802 CRC32

External Memory Interface (EMI)

- 8 MB memory space
- Support 4 pages

SDRAM Controller

- Support 16Mb/64Mb/128Mb/256Mb

LCD Controller

- Configurable pixel clock frequency
- RGB888 color data parallel or serial output
- RGB666 color data parallel output
- RGB color data serial output order configurable
- Three internal high speed video DAC can output analog R/G/B colors
- Hardware OSD support
- Video data stored in SRAM can be in packaged mode or planner mode
- LCD panel size support up to 1024x768 pixels
- Hardware YUV2RGB converter

USB OTG Full Speed Controller

- Support 4 endpoints
- Total FIFO size is 512 bytes

A/D Converter (ADC)

- 8 channels
- 10-bit resolution

Peripherals

- Digital tuning system (DTS)
- RTC
- AUDIO DAC
- SD HOST CONTROLLER
- SPI
- UART
- IIS
- GPSI
- WDT
- ECC for NAND FLASH

Development and Debug

- GCC compiler toolset
- On-line debugging through IEEE 1149.1 JTAG protocol and GDB

Package Type

- LQFP 128-pin
- LQFP 144-pin

Temperature

- Operating temp.: -40°C to +85°C
- Storage temp.: -65°C to +150°C

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