



# AX3005 MP3/WMA Decoder SoC



## High Performance 32-bit RISC CPU

- 32-bit OpenRISC CPU running at up to 120MIPS
- 12KB Mask ROM for system booting
- 104KB on-chip SRAM for MP3/WMA decoder
- 23 vectored interrupt controller with two-level programmable interrupt priority
- Debug interface connects to GDB via JTAG
- Internal 32-bit ticker-tick timer

## Hardware Accelerate Unit

- 5-channel general purpose DMA controller

## Internal Arithmetic Unit

- Powerful ECC arithmetic for NAND flash memory by EMI interface
- 16-bit DSP engine

## Serial Interface

- High-speed full-duplex UART with baud rate generator
- Two SPI with double buffer, operates up to 24Mb/s
- Dual channel 32-bit IIS for audio codec
- USB 2.0 OTG controller with 512 bytes FIFO
- SD card interface for SDHC specification 2.0
- GPSI

## Power Saving mode

- Idle
- Stop
- Sleep

## Other Peripherals

- 53 (80 pins), 43 (64pins) GPIO with configurable pull-up resistors 8mA driving ability
- 8 channel ADC with 10-bit conversion precision
- 4 16-bit Multi-Function timers can be configured to timer, counter, capture, PWM mode
- Internal DTS to connect FM/AM transceiver IC
- Watchdog Timer clocked from with on-chip RC oscillator
- 4-20MHz crystal oscillator
- 1.6MHz embedded RC oscillator
- 32.768KHz Real-time oscillator
- Phase lock loop for maximum 200MHz clock generation
- Power-on reset
- Low voltage detector
- On-chip regulator for 3.3V to 1.8V conversion
- Two dual channel 16-bit audio DACs (One with class-D AMP)
- External interrupt for system wakeup from power save mode

## Development and Debugging support

- GCC compiler toolset
- On-line debugging through IEEE 1149.1 JTAG protocol and GDB

## Packages

- 64-pin LQFP
- 80-pin LQFP



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