



US005949728A

United States Patent [19]

[11] Patent Number: **5,949,728**

Liu et al.

[45] Date of Patent: **Sep. 7, 1999**

[54] **HIGH SPEED, NOISE IMMUNE, SINGLE ENDED SENSING SCHEME FOR NON-VOLATILE MEMORIES**

5,386,388	1/1995	Atwood et al.	365/201
5,410,511	4/1995	Michiyama	365/218
5,477,499	12/1995	Van Buskirk et al.	365/218
5,521,875	5/1996	Callahan	365/207
5,559,737	9/1996	Tanaka et al.	365/185.25
5,563,843	10/1996	Fackenthal et al.	365/233.5
5,608,675	3/1997	Nam	365/207
5,625,588	4/1997	Seyyed et al.	365/207

[75] Inventors: **Kwo-Jen Liu**, San Jose; **Chuck Cheuk-Wing Cheng**, Saratoga, both of Calif.

[73] Assignee: **Scenix Semiconductor, Inc.**, Santa Clara, Calif.

Primary Examiner—Tan T. Nguyen
Attorney, Agent, or Firm—Fenwick & West LLP

[21] Appl. No.: **08/989,936**

[57] **ABSTRACT**

[22] Filed: **Dec. 12, 1997**

A single ended sensing scheme amplifies the logic state stored within a non-volatile memory circuit by relying upon three stages, a clamping circuit, a first operational amplifier and a second operational amplifier. The clamping circuit clamps the voltage at a voltage level with a small voltage swing between the logic states. The first stage and second stage operational amplifiers increase the clamped voltage level. A reference memory circuit ensures that the sensing scheme output is properly adjusted to compensate for voltage and temperature variations as well as noise injection from the power supply and ground.

[51] Int. Cl.⁶ **G11C 7/00**

[52] U.S. Cl. **365/206; 365/189.06; 365/210**

[58] Field of Search **365/206, 207, 365/189.06, 210, 211, 185.21**

[56] References Cited

U.S. PATENT DOCUMENTS

4,594,689	6/1986	Donoghue	365/182
4,918,341	4/1990	Galbraith et al.	365/207
5,013,943	5/1991	Hirose	307/530
5,117,394	5/1992	Amin et al.	365/203

20 Claims, 3 Drawing Sheets

