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Cheng

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(54) **SINGLE CYCLE TRANSITION PIPELINE PROCESSING USING SHADOW REGISTERS**

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(57) **ABSTRACT**

A system and method for efficiently handling interrupts in a microcontroller environment is disclosed. An interrupt handling circuit preserves a current state of a microcontroller comprising a plurality of primary registers for storing information relating to the current state of the microcontroller and a plurality of shadow registers coupled to at least two of the primary registers for storing the information contained in an interrupt enter signal from an interrupt signal generator. In one embodiment the information relating to the current state of the microcontroller includes the program counter, accumulator data, CPU status data, and an address pointer to data memory. In a preferred embodiment, the information is restored to the primary registers within one clock cycle of receiving an interrupt exit signal from the interrupt signal generator. In a pipeline stage embodiment a sequence of interrupt instructions is fed into the pipeline in subsequent clock cycles after the data is stored in the shadow registers, facilitating a rapid response to the interrupt.

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(51) **Int. Cl.**⁷ **G06F 9/48**

(52) **U.S. Cl.** **712/228; 709/108; 710/260; 712/229; 712/244**

(58) **Field of Search** **710/260; 712/228, 712/229, 244; 709/108**

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4 Claims, 7 Drawing Sheets

