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**Cheng**

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(54) **FOUR STAGE PIPELINE PROCESSING FOR A MICROCONTROLLER**

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(57) **ABSTRACT**

A system and method for efficiently processing instructions in a pipeline architecture for a microcontroller and maintaining a fixed instruction execution per clock cycle rate is disclosed. The pipeline comprises four stages: an instruction fetch stage, an operand fetch stage, an execution stage, and a write back stage. In a first embodiment, an entire clock cycle is dedicated to the instruction fetch stage to retrieve instruction data from non-volatile memory in a single clock cycle. In a second embodiment, the operand fetch stage preliminarily decodes the instruction data to determine tasks to be performed to allow the execution stage to perform its time-intensive calculations in a single clock cycle. Additionally, the operand fetch stage initiates the performance of tasks determined from the decoding of the instructions to minimize the time required to perform those tasks by the execution stage. In one embodiment, a read address is generated responsive to determining that a read operation is to be performed by the execution stage. In a third embodiment, a dual port data memory is employed to allow the execution stage and the write back stage to perform read and write operations concurrently, in a single clock cycle. Additional embodiments are disclosed for addressing circumstances in which one stage modifies the data address pointer required by another stage or one stage writes to an data memory location required for a read operation by a previous stage. Thus, a one instruction per clock cycle rate is achieved and maintained.

**2 Claims, 9 Drawing Sheets**

